Claims

[c1] 1. A content addressable memory (CAM), comprising:

an input circuit suitable for presenting input data to a plurality of cell circuits;

a match circuit including a match-high line, a match-low line, and a pre-charge sub-circuit able to controllably connect said match-high line to a voltage source and to controllably connect said match-low line to a ground, thereby charging said match-high line and discharging said match-low line; and

said plurality of cell circuits each able to compare one bit of said input data with one bit of pre-stored storage data to determine whether pre-specified match criteria are met, and to operationally connect said match-high line and said match-low line if said match criteria are met, thereby permitting detection of a mismatch condition.

[c2] 2. The CAM of claim 1, further comprising a clock suitable for cycling at a clock frequency, and wherein:

said plurality of cell circuits each perform one comparison per cycle of said clock; and

said pre-charge sub-circuit connects said match-high line to said voltage source and said match-low line to said ground at half of said clock frequency.

[c3] 3. The CAM of claim 1, wherein said match criteria define a binary mode comparison between said one bit of said input data and said one bit of pre-stored storage data.

[c4] 4. The CAM of claim 1, wherein said match criteria define a ternary mode comparison between said one bit of said input data, said one bit of pre-stored storage data, and one bit of pre-stored mask data.

[c5] 5. The CAM of claim 1, wherein said input circuit controllably specifies whether said match criteria define a binary mode comparison or a ternary mode comparison.

[c6] 6. The CAM of claim 1, wherein a plurality of said plurality of cell circuits define rows such that each said row has a respective common said match circuit, thereby permitting comparison of said input data and a plurality of instances of said pre-stored storage data.

[c7] 7. A method for comparing input data with pre-stored storage data in an associative manner, the method comprising the steps of:

(a) pre-charging a match-high line to a high state and a match-low line to a low state;

(b) presenting the input data to a plurality of cell circuits;

(c) comparing one bit of the input data with one bit of the pre-stored storage data in each of said plurality of cell circuits to determine whether pre-specified match criteria are met; and

(d) connecting said match-high line and said match-low line if said match criteria are met, thereby permitting detection of a mismatch condition.

[c8] 8. The method of claim 7, wherein:

said step (c) occurs at a clock frequency; and

step (a) includes pre-charging said match-high line and said match-low line at half of said clock frequency.

[c9] 9. The method of claim 7, wherein said step (c) includes binary mode comparison between said one bit of the input data and said one bit of the pre-stored storage data.

[c10] 10. The method of claim 7, wherein said step (c) includes ternary mode comparison between said one bit of the input data, said one bit of the pre-stored storage data, and one bit of pre-stored mask data.

[c11] 11. The method of claim 7, further comprising (e) specifying whether said match criteria define a binary mode comparison or a ternary mode comparison.

[c12] 12. A content addressable memory (CAM) for binary mode comparison of input bits with storage bits, comprising:

an input circuit suitable for presenting the input bits to a plurality of cell circuits;

a match circuit including a match-high line, a match-low line, a pre-charge sub-circuit able to controllably bring said match-high line to a high state and said match-low line to a low state, and a plurality of match-gates at least equaling said plurality of cell circuits, wherein each said match-gate is able to operationally connect said match-high line with said match-low line in response to a match signal; and

said plurality of cell circuits each suitable for:

storing one of the storage bits; and

generating a said match signal based on the states of the input bit and its storage bit, thereby permitting the CAM to compare the input bits with the storage bits to detect a mismatch condition.

[c13] 13. The CAM of claim 12, further comprising a clock suitable for cycling at a clock frequency, and wherein:

said input circuit presents the input bits to said plurality of cell circuits at said clock frequency; and

said pre-charge sub-circuit operates at half of said clock frequency.

[c14] 14. The CAM of claim 12, wherein a plurality of said plurality of cell circuits define rows such that each said row has a respective common said match circuit, thereby permitting comparison of said input data and a plurality of instances of said storage data.

[c15] 15. A method for comparing input bits with storage bits in a binary associative manner, the method comprising the steps of:

(a) pre-charging a match-high line to a high state and a match-low line to a low state;

(b) storing each of the storage bits in a respective memory cell;

(c) generating respective match signals based on the states of the input bits and said memory cells; and

(d) connecting said match-high line and said match-low line responsive to any one of said match signals, thereby comparing each of the input bits with each of the storage bits to detect a mismatch condition.

[c16] 16. The method of claim 15, wherein:

said step (c) occurs at a clock frequency; and

said step (a) occurs at half of said clock frequency.

[c17] 17. A content addressable memory (CAM) for ternary mode comparison of input bits with storage bits and mask bits, comprising:

an input circuit suitable for presenting the input bits to a plurality of composite cells;

a match circuit including a match-high line, a match-low line, a pre-charge sub-circuit able to controllably bring said match-high line to a high state and said match-low line to a low state, and a plurality of match-gates at least equaling said plurality of cell circuits, wherein each said match-gate is able to operationally connect said match-high line with said match-low line in response to a match signal; and

said plurality of composite cells each suitable for:

storing one of the storage bits and one of the mask bits as a ternary unit having three possible states (1, 0, and X, wherein X represents masked); and

generating a said match signal based on the states of the input bit and said ternary unit, thereby permitting the CAM to compare one of the input bits with one of the storage bits and one of the mask bits to detect a mismatch condition.

[c18] 18. The CAM of claim 17, further comprising a clock suitable for cycling at a clock frequency, and wherein:

said input circuit presents the input bits to said plurality of composite cells at said clock frequency; and

said pre-charge sub-circuit operates at half of said clock frequency.

[c19] 19. The CAM of claim 17, wherein a plurality of said plurality of cell circuits define rows such that each said row has a respective common said match circuit, thereby permitting comparison of said input data and a plurality of instances of said storage data.

[c20] 20. A method for comparing input bits with storage bits and mask bits in a ternary associative manner, the method comprising the steps of:

(a) pre-charging a match-high line to a high state and a match-low line to a low state;

(b) storing the storage bits and the mask bits in composite cells as a ternary units having one of three possible states (1, 0, and X, wherein X represents masked);

(c) generating respective match signals based on the states of the input bits and said composite cells; and

(d) connecting said match-high line and said match-low line responsive to any one of said match signals, thereby comparing each of the input bits with each of the storage bits to detect a mismatch condition.

[c21] 21. The method of claim 20, wherein:

said step (c) occurs at a clock frequency; and

said step (a) occurs at half of said clock frequency.

[c22] 22. A content addressable memory (CAM) for comparison of a data set in either binary mode or ternary mode, comprising:

an input circuit suitable for presenting input bits from the data set to a plurality of composite cells;

a match circuit including a match-high line, a match-low line, a pre-charge sub-circuit able to controllably bring said match-high line to a high state and said match-low line to a low state, and a plurality of match-gates at least equaling said plurality of composite cells, wherein each said match-gate is able to operationally connect said match-high line with said match-low line in response to a match signal; and

said plurality of composite cells each suitable for selective operation in either the binary mode or the ternary mode, wherein:

in the binary mode each said composite cell is suitable for:

storing two storage bits;

receiving two said input bits from said input circuit; and

generating two said match signals respectively based on the states of a said input bit and a said storage bit, thereby permitting the CAM to compare the data set with said storage bits in binary manner to detect a mismatch condition; and

in the ternary mode each said composite cell is suitable for:

storing one storage bit and one mask bit as a ternary unit having three possible states (1, 0, and X, wherein X represents masked);

receiving one said input bit from said input circuit; and

generating a said match signal based on the states of said input bit and said ternary unit, thereby also permitting the CAM to compare the data set with said storage bits and said mask bits in ternary manner to detect a mismatch condition.

[c23] 23. The CAM of claim 22, further comprising a clock suitable for cycling at a clock frequency, and wherein:

said input circuit presents said input bits to said plurality of composite cells at said clock frequency; and

said pre-charge sub-circuit operates at half of said clock frequency.

[c24] 24. The CAM of claim 22, wherein a plurality of said plurality of composite cells define rows, thereby permitting comparison of said data set with a plurality of sets of said storage bits in the binary mode and with a plurality of sets of said storage bits and said mask bits in the ternary mode.

[c25]

25. A method for comparison of a data set in either binary or ternary associative manner, the method comprising the steps of:

(a) pre-charging a match-high line to a high state and a match-low line to a low state;

(b) selecting operation in either the binary mode or the ternary mode;

(c) in the binary mode:

(1) storing two storage bits in a composite cell

(2) selecting two input bits from the data set; and

(3) generating a match signal based on the states of said input bits and said storage bits; and

(d) in the ternary mode:

(1) storing a storage bit and a mask bit in said composite cell as a ternary unit having one of three possible states (1, 0, and X, wherein X represents masked);

(2) selecting one input bit from the data set; and

(3) generating said match signal based on the states of said input bit and said ternary unit; and

(e) connecting said match-high line and said match-low line responsive to any one of said match signals, thereby permitting the CAM to compare the data set with said storage bits in binary manner to detect a match and to also compare the data set with said storage bits and said mask bits in ternary manner to detect a mismatch condition.

[c26] 26. The method of claim 25, wherein:

said step (c)(3) and said step (d)(3) occur at a clock frequency; and

said step (a) occurs at half of said clock frequency.